3.1 Test circuits

Figure 2. **Test circuit**

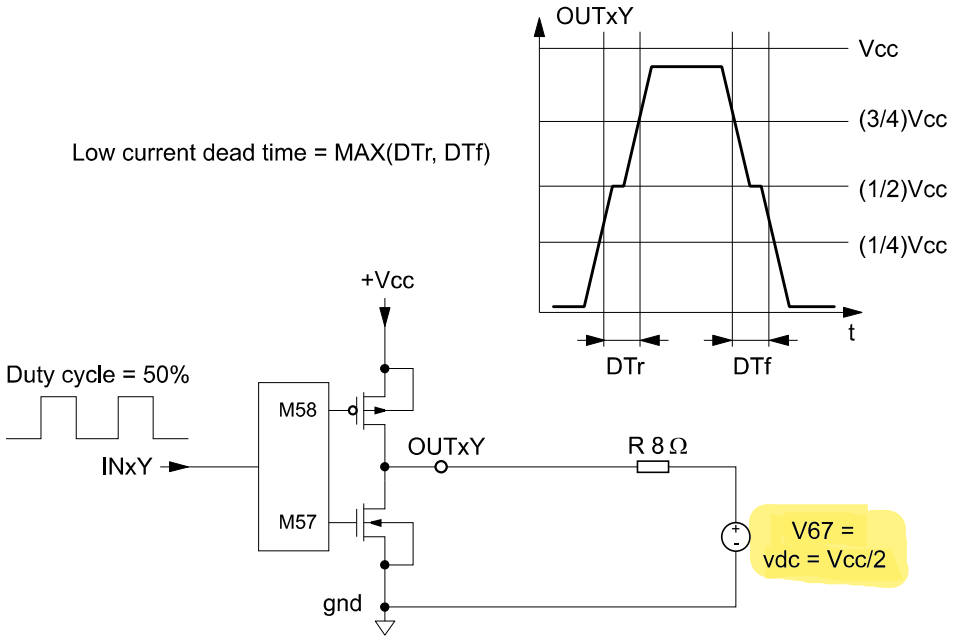

Figure 3. **Current dead-time test circuit**