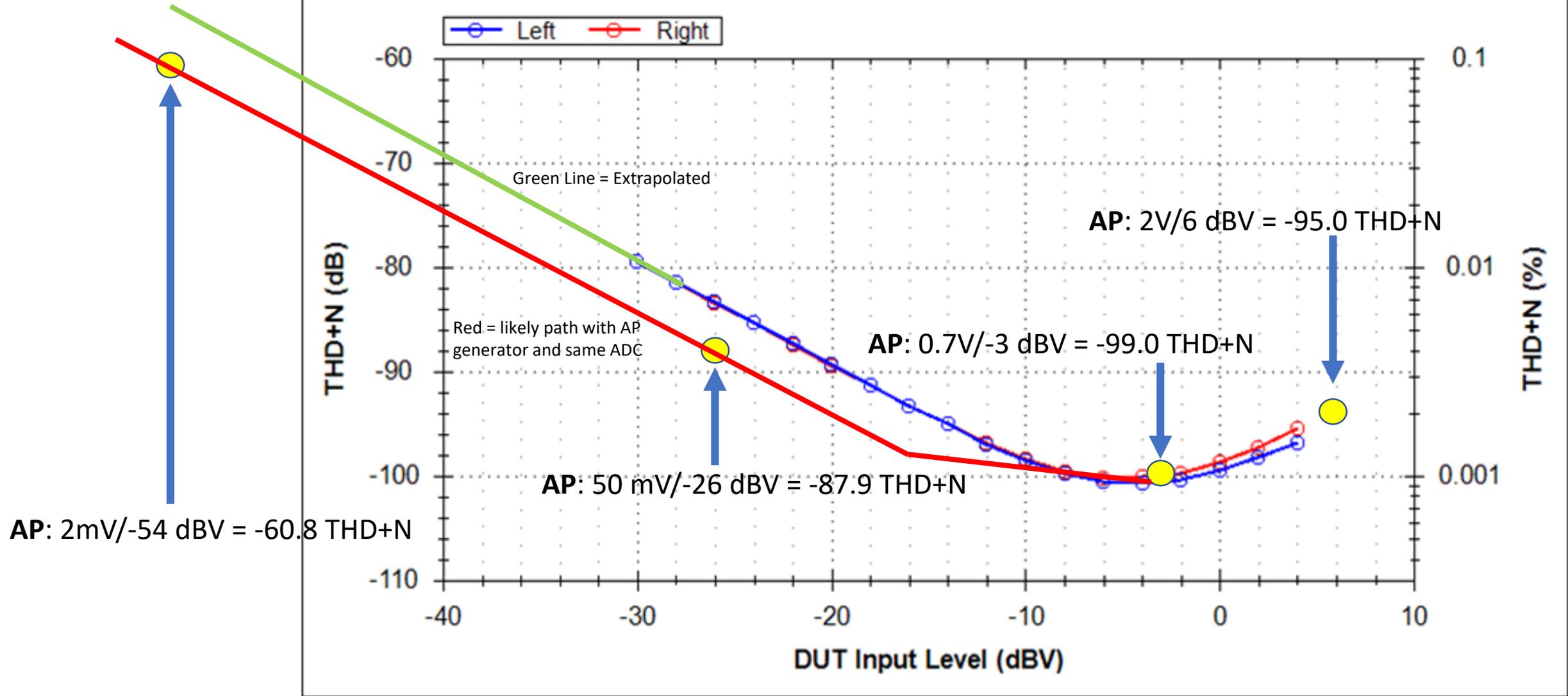
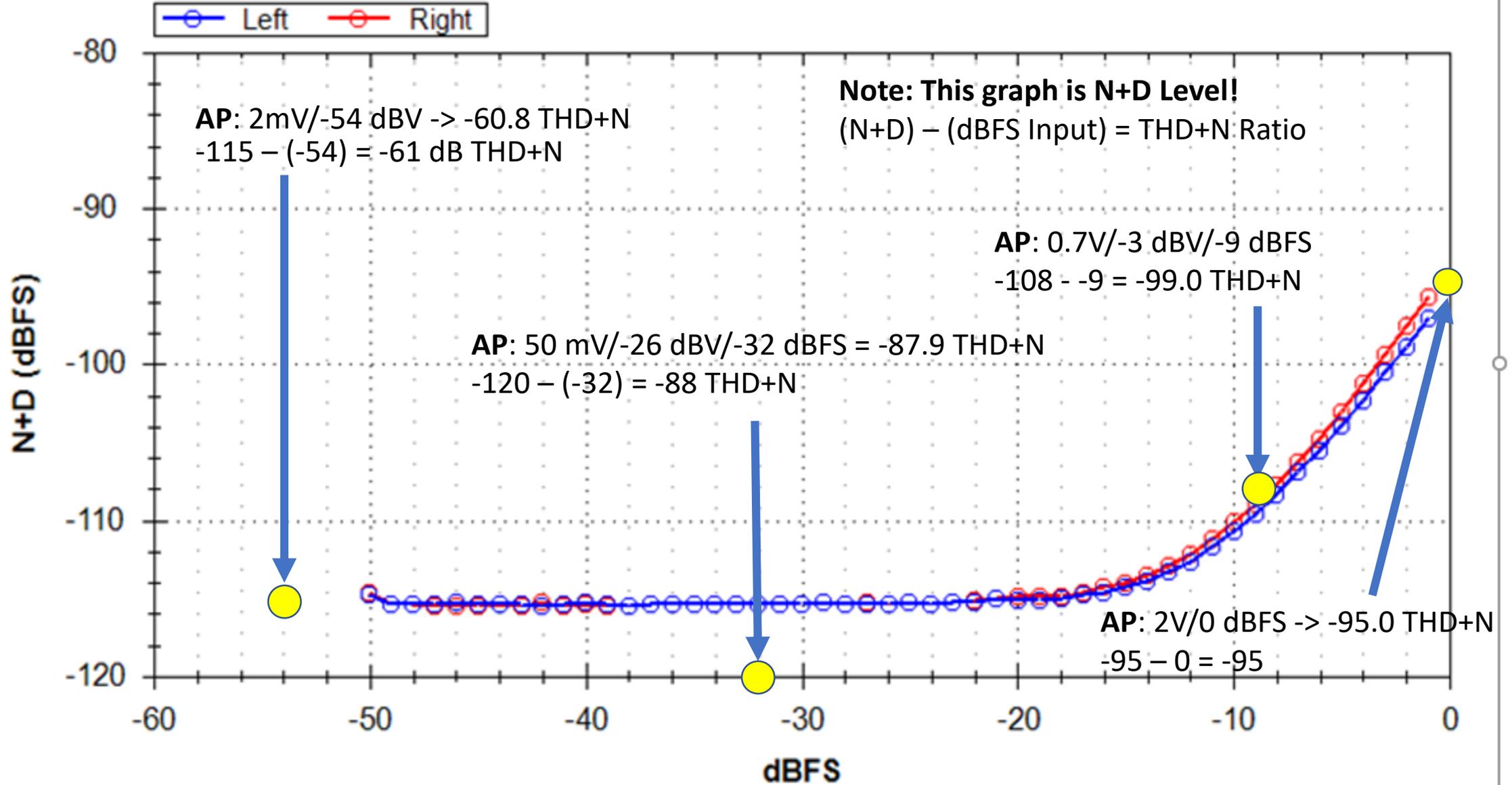


# Unit JNB THD+N versus Level



# Unit JNB N+D versus Input Level





QA401 in loopback at max and reduced output level

Yellow = 1.874Vrms = 5.45 dBV

Green = -60 dBV (relative to 5.45 dBV)

Take away here is that noise floor change between max signal and -60 dBFS signal is about 8 dB

These should be repeatable on any QA401 in similar config



QA401 Loopback (yellow) and input shorted (green)

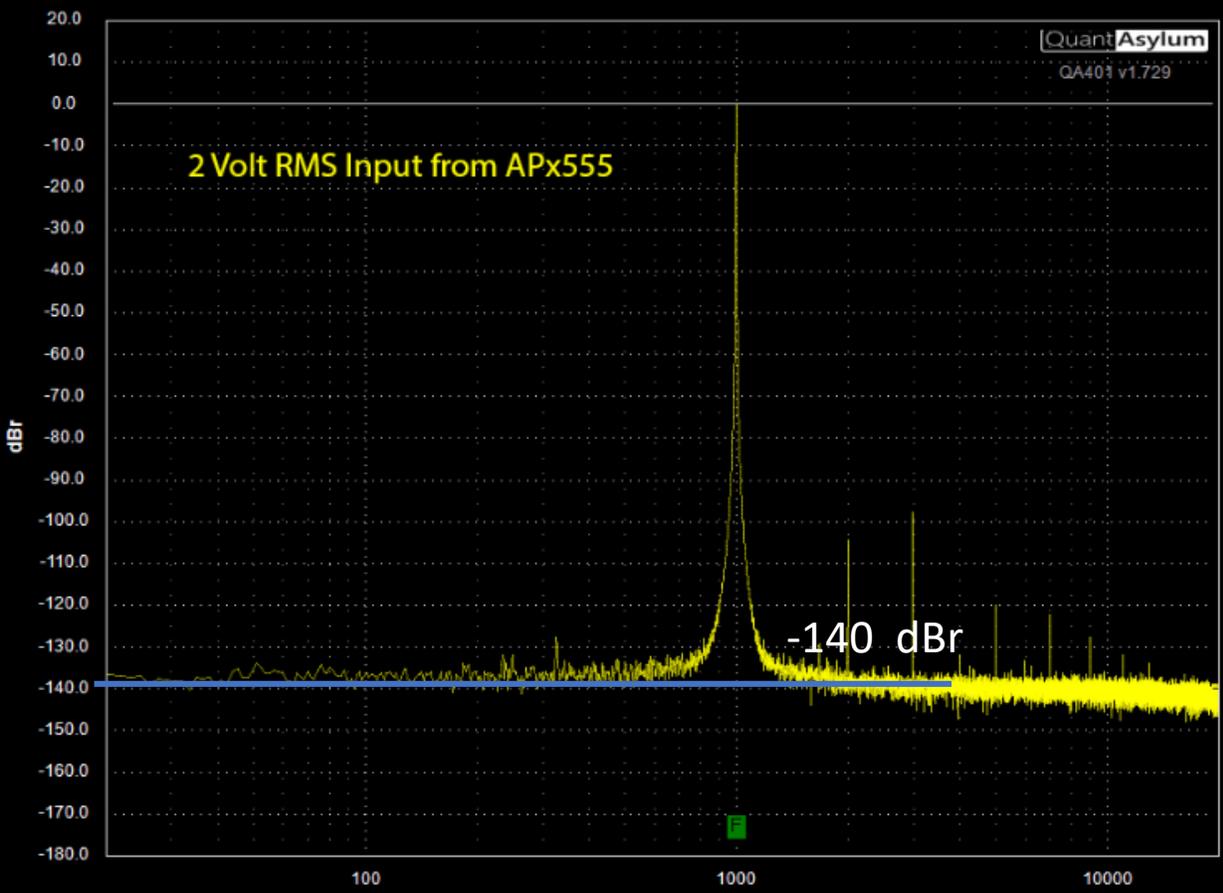
Yellow = 1.874Vrms = 5.45 dBV

Green = Input Shorted

Take away here is that the as the generator quality improves, the gap will grow (here it is 13 dB).

This is true for ALL analyzers, up to the dynamic range of the analyzer. IOW if the source is better than the analyzer's own generator, then the noise floor gap will increase

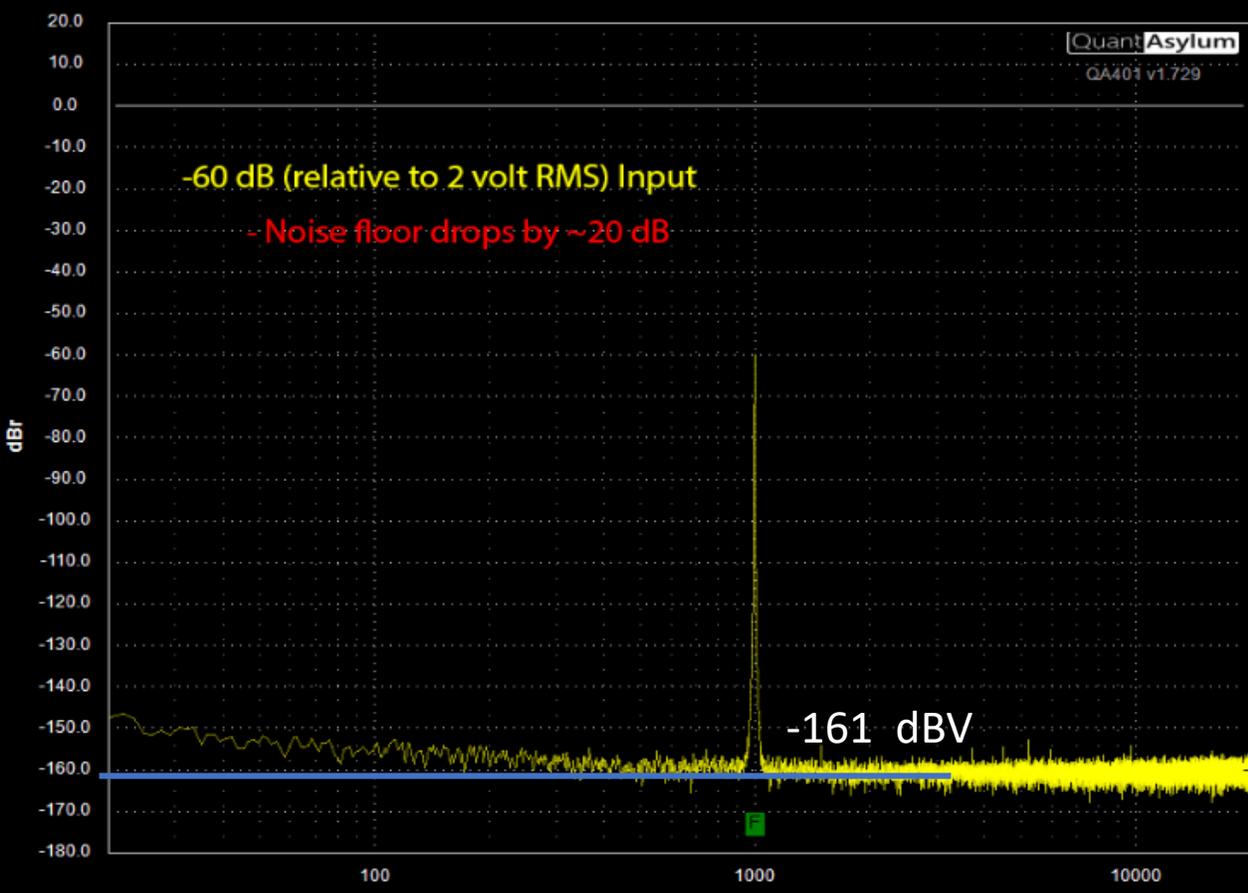
FFT: 32768 pts    Meas Start: 20.0 Hz    Peak L: 0.01 dBr    Gen 1: 1.000488 KHz @ -9.5 dBr  
 Avg: 8    Meas Stop: 20.0 KHz    RMS L: 0.5 dBr    Gen 2: 19.99951 KHz @ -19.6 dBr  
 Res: 1.46 Hz    RMS L: 0.5 dBr    Peak L: 1.885 Vrms  
 Fs: 48.0 KHz    N+D L: -95.2 dBr    THD L: -97.0 dB/ 0.00142%    THD+N L: -95.2 dB/ 0.00173%  
 Win: Hann  
 Weight: None



QA401 being fed from AP at same level as previous slide. But this time, the noise is -140 dBr versus -148 dBr. It grew! How??! More on that in a bit...

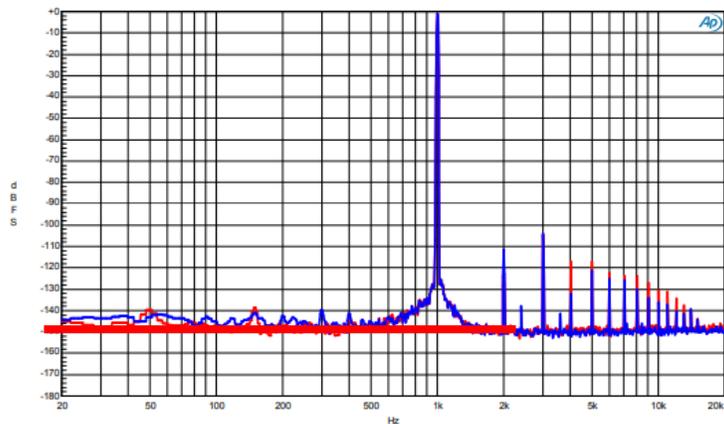
Total Gap is 21 dB

FFT: 32768 pts    Meas Start: 20.0 Hz    Peak L: -60.00 dBr    Gen 1: 1.000488 KHz @ -9.5 dBr  
 Avg: 8    Meas Stop: 20.0 KHz    RMS L: -59.5 dBr    Gen 2: 19.99951 KHz @ -19.6 dBr  
 Res: 1.46 Hz    RMS L: -59.5 dBr    Peak L: 1.884 mVrms  
 Fs: 48.0 KHz    N+D L: -120.8 dBr    THD L: -84.9 dB/ 0.00571%    THD+N L: -60.8 dB/ 0.09145%  
 Win: Hann  
 Weight: None

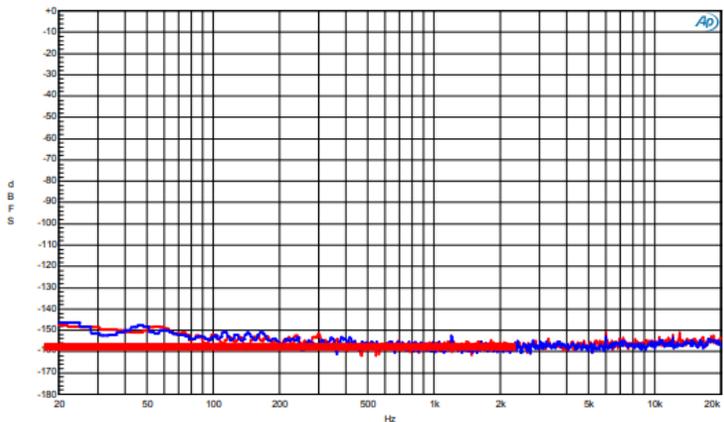


This is same noise floor as QA401 with input shorted. Conclusion is that AP generator has a noise floor below that of the QA401 input, which is to be expected

fs = 48 kHz  
 AK5397 FFT (-1dBFS Input)  
 AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz



fs = 48 kHz  
 AK5397 FFT (No Signal Input)  
 AVDD=5.0V, DVDD=3.3V, VREFL+/-=VREFR+/-=5.0V/VSS, MCLK=512fs, fin=1kHz

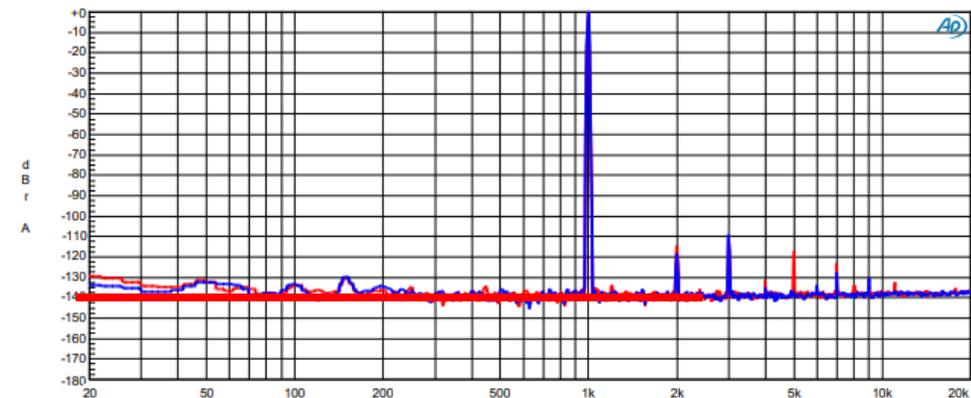


ADC shows a change in noise floor of ~10 dB between max signal and idle

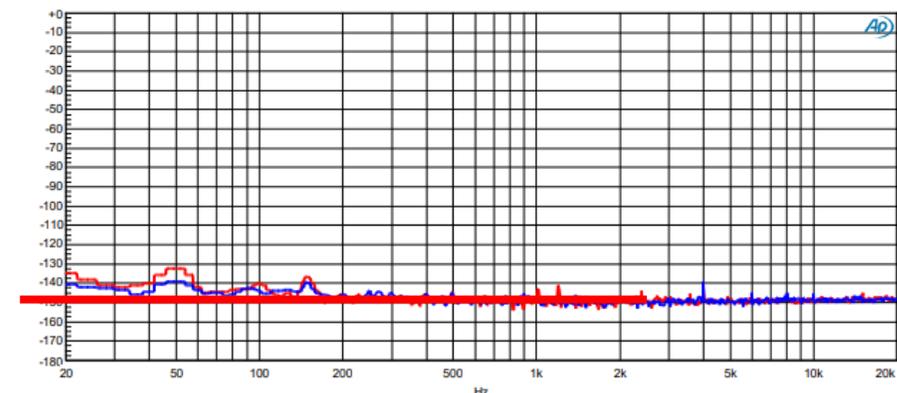
Data from AKM EVM Reports.

Takeaway from this slide is that there's a ~10 dB change in noise floor based on input level

AKM  
 AK4490 FFT (0dBFS Input)  
 AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz



AKM  
 AK4490 FFT (No Signal Input)  
 AVDD=DVDD=3.3V, VDDL/R=VREFHL/R=5V, MCLK=512fs, fs=44.1kHz



DAC shows a change of ~10 dB between max signal and idle. But note if ADC and DAC max signals are equal, then DAC noise dominates by about 10 dB. In other words, DAC is limiting factor

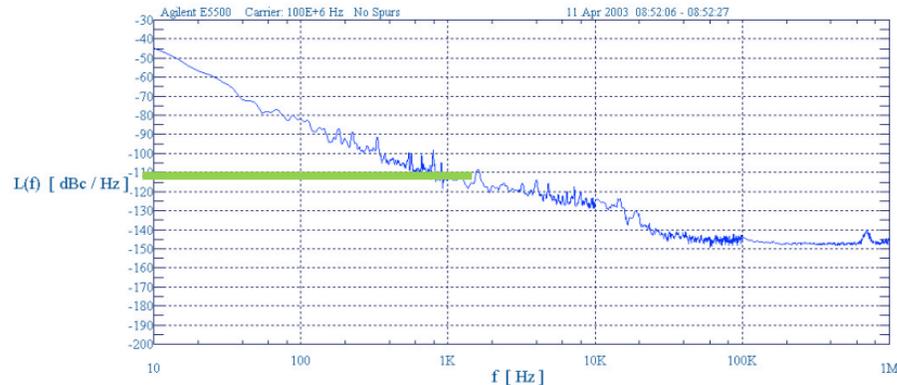
# OK, so what about the noise gap?

- For the case of loopback (8 dB gap)...
  - This is overwhelmingly from the ADC/DAC (see previous slide). This is the norm for all sigma delta. You can hide this by giving up dynamic range.
- For the case of loopback versus shorted input (13 dB gap)...
  - ~8 dB of this from the DAC
  - ~5 dB of this is from the elimination of the DAC's idle noise (by shorting input)
- For the case of AP into QA401 (21 dB gap)
  - ~8 dB is from the DAC
  - ~5 dB is from the killer noise floor of the AP generator
  - This leaves about 8 dB of noise INCREASE that needs to be explained

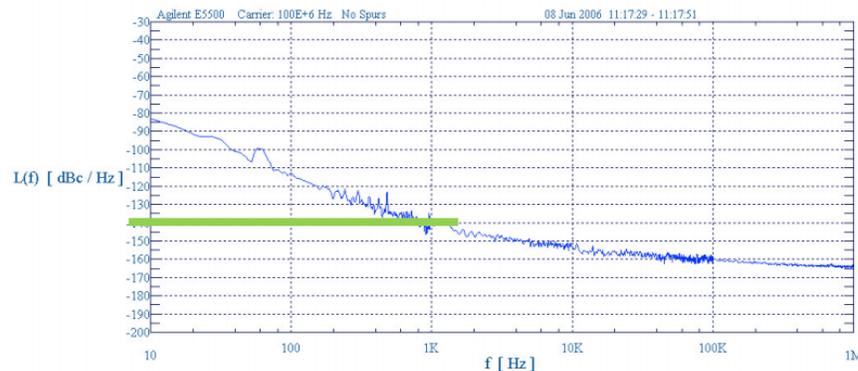
# Explaining the last 8 dB...

- This gets tricky, because it caused the floor to rise at max signal input
  - Noise floor at max input went from -148 (driven by QA401) to -140 (driven by AP).
- The most likely explanation here would be a difference in phase noise
  - When the QA401 is measuring a signal derived from its own clock, then phase noise is zero.
- The QA401 uses a \$2 oscillator. We'd expect a piece of \$30K test equipment to use an ultra-low phase noise oscillator that costs between \$20 and \$200

# From A Crystek App Note



**Figure 6.** SSB phase noise plot of a commodity clock.



**Figure 7.** SSB phase noise plot of a true ultra-low phase noise oscillator (model: Crystek CCHD-950).

- Roughly, the close-in phase noise between a commodity oscillator and an ultra-low-noise phase oscillator might be around 30 dB
- 30 dB is huge...
- The phase noise translate to jitter.
- And the jitter (if random) translate to noise floor (if not random it can translate to tones)
- But the path above is complex and often very speculative unless you have extremely precise measurements to guide your way.

# So, what about “noise modulation”?

- All sigma delta converters exhibit a changing noise levels based on input level.
  - But that change is small (usually <10 dB) and becomes more pronounced near max input
  - And that change isn't generally the limiting factor in THD+N—that limit comes purely from harmonics
  - While this could loosely be considered “noise modulation,” noise modulation more commonly refers to the processing that takes quantization noise and moves it outside the band of interest.
- Additional changes to noise levels (versus loopback) can come from two (or more) places:
  - Via a reduction in noise floor, if the DUT has a noise floor much lower than the analyzer
  - Via increase in noise floor, if the DUT has a substantially better or worse phase noise than the analyzer.